Fast PC & CAMAC Based Multiparametric Acquisition System

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We have developed a PC-based data-acquisition system for use in making accurate branching-ratio measurements for superallowed Fermi beta decays. The system is required to be fast, with a short, well controlled dead-time. As described in [1] the basic parameters defining an event are triplets of the form γ–β_1–$\overline{\beta}_2$: that is, gamma rays from a HPGe detector in coincidence with betas from one plastic-scintillator / phototube detector and in anti-coincidence with betas from the other. We use the beta-gamma coincidence technique to eliminate gamma-ray background and clean the gamma spectra from unwanted beta events.

A multi-parametric acquisition system based on KmaxNT software [2] and on CAMAC modules with FERA readout has been developed. The system hardware includes analog-to-digital converters (ADC: EG&G Ortec, model AD413A; QDC: LeCroy, model 4300B; TDC: LeCroy, model 3377), a FERA driver (LeCroy, model 4301), two dual port FERA/CAMAC buffer-memories (LeCroy 4302), a controller with SCSI capability (SPARROW SCM301) and a 330MHz PC, operating in the WindowsNT environment. The data flow from the primary electronics to the computer occurs in two distinct steps. In the first one, the data are transferred on the FERA bus from the converters to the memories. In the second step, a buffered-mode data transfer takes place from the memories to the PC.

The multi-parametric buffered acquisition, which was originally proposed by the supplier of the KmaxNT software, Sparrow "Hawk_MPB.tsh" [2], makes use of a "ping-pong" selection scheme of the two memories, the selection being driven by the PC. During the time that one memory is set in FERA mode (ready to receive data from the converters), the other one is set in CAMAC mode and its information is transferred to the PC; when the memory in FERA mode reaches a preset limit, it will issue a LAM signal which will result in a swap of the two memories. This is not satisfactory for our purposes since such a procedure introduces an undesired and uncontrolled dead-time associated to the interaction between the NT machine and the CAMAC controller. A command sent by the NT machine to the CAMAC controller needs a minimum of 250 μs, a maximum of 480 μs and a mean time of about 300 μs. Because the controller cannot initiate a data transfer, the PC polls the controller periodically. Under these circumstances, each "polling & command-sending" sequence also introduces a dead-time in the range of about 4.4 ms to 6.5 ms with a mean value of about 4.45 ms. (These values were measured in the absence of any network interaction of the PC.)

In order to avoid those dead-time problems, we developed a new method to swap the memories by making use of a Jorway 221 CAMAC module. The Jorway unit sends out two logic signals that flip-flop from one to the other. They are used to veto each memory alternately. The two memories are set in the FERA mode as a "normal" state and thus record data unless they have been vetoed. The period for alternation of

these logic signals is adjustable via software and is always set in advance of final data-taking to be less than the time necessary to fill a memory under the prevailing experimental conditions.

The normal readout of the memories had to be modified as well, since a LAM signal issued by the memories cannot be correlated with the Jorway-imposed swapping period. Thus, we initiate one memory read-out by a LAM signal issued from the Jorway unit at the beginning of each veto cycle and the other, 50 μs after the half period. This delay was chosen for safety and convenience, as the period is normally in the range of 0.2 s to 8.0 s. Thus, our acquisition system introduces essentially no extra dead time relative to that corresponding to the converters. Our procedure reduces the dead time associated with the memory-swap to 2 μs, a time during which both memories are vetoed.

Another feature of our acquisition system is the use of converters with widely differing conversion times. This added a problem of incompatibility among the individual gate requirements of the various modules in the coincidence scheme. For example, the QDC (used for fast beta signals from the phototube) requires a fast and short gate, whereas the ADC (used for the slow gamma-ray signals from the HPGe detector) demands delayed and long gates relative to the time of the fast coincidence between the β and γ-ray signals. We solved this problem by breaking the "gate line" in the command bus controlled by the FERA driver and introducing well adjusted gate signals with the corresponding termination for each individual converter.

References

1. J.C. Hardy, V.E. Iacob, A. Azhari, V.V. Baturin, R. Burch, C.A. Gagliardi, P. Lipnik, E. Mayes, L. Trache and R.E. Tribble, Progress in Research 1998-1999, *Cyclotron Institute*, TAMU.
2. See "http://sparrowcorp.com"